BL310

I2C VERSATILE RELAY DRIVER

Features

- Addressable Relay drive
- Single-coil Latching and Normal relays
- Low power
- Drives 1 to 8 relays per IC
- Up to 100 relays per I2C address
- Direct drive of low power relays
- Non-volatile storage of relay state
- Programmable power-on state
- Small parts count
- 5V operation.
- Low cost

Applications

- Instruments
- ATE multiplexors
- low-power equipment
- Rapid Prototyping & PnP design
- Server power and network failsafe switches

Programmable

EEProm stores commands and settings

- Base I2C Address
- Settings

Description

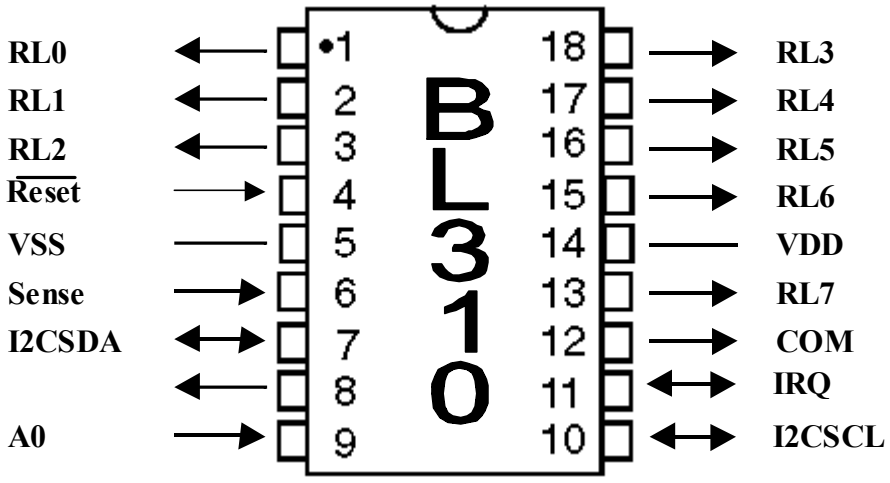
The BL310 directly drives from 1 to 8 low power relays.
Single coil Latching relays are directly driven with the set and reset pulse sequencing taken care of by the IC.

As well as being an I2C addressable relay driver, it can also be used as simple logic to latching relay converter where low power drain is needed

The state of the relays can be stored. This means that normal[1] relays can be made to latch, or that the state of latching relays is known after a power interruption.

8 low power latching relays can be directly driven. Typical types are the NAIS TQ2L small signal relays and ADJ series 16A switching relays.
High coil currents can be driven by a single external SOT563 transistor per relay.

Unused outputs can be used as general purpose I/O.
Pre-built modules are available for rapid prototyping.



[1] Normal relays are also known as single-side stable

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1 Table 1: BLXXX Pinout Description

Name	DIP Pin #	SSOP Pin #	I/O/P Type	Buffer Type	User Pin	Description	bit #
	1	1	I/O	TTL	I/O		
	2	2	I/O	TTL	I/O		
	3	3	I/O	ST	I/O		
Reset	4	4	In	ST	In		
VSS	5	5,6					
Int	6	7	In	ST	I/O	0=interrupt	
SDA	7	8	In	ST[2]	--		
	8	9	Out		--		
A0	9	10	In	TTL	I/O	3 level pin VDD, GND, 100k-gnd	
SCL	10	11	I/O	ST	I/O		
	11	12	I/O	TTL	I/O		
	12	13		TTL	I/O		
	13	14		TTL	I/O		
VDD	14	15,16					
	15	17		ST	O		
	16	18		CMOS	I/O		
	17	19	I/O	TTL	I/0	E	
	18	20	I/0	TTL	I/0		

2 Circuit Operation

3 I2C Bus

3.1 Write Operations

[Start] [I2CAddress][RegisterAddress/Command][data 1..n]

3.2 Read Operations

3.3 Bit Timing

Both standard 100kHz, and fast 400kHz I2C Timing is supported.

3.4 SCL Stretch

SCL Stretch is used. The slave holds SCL low to assert stretch after the ACK.
Your bus master should check SCL at the *start* of each byte/Start/stoP. If you do this SCL stretch will probably not impact. By testing at the beginning of the next byte, most SCL stretches will have no affect on throughput.
SCL Stretch is asserted for a max of ??? µs

3.5 Thresholds

SCL and SDA have Schmitt trigger inputs.

[2] Schmitt Trigger

3.6 I2C Addresses

7 bit I2C addressing only is supported.
Address pins A0 is a 3 level input used to select 1 of 3 addresses. The third state R0 is a 100k resistor to VSS. Note that you can leave the pin open for VDD as an internal pullup is active.

Address Pin Selection									
Base+	0	1	2	3	4	5	6	7	8
A0	VSS	VDD	RG	VSS	VDD	RG	VSS	VDD	RG
A1	VSS	VSS	VSS	VDD	VDD	VDD	RG	RG	RG

3.6.1 Programmable Addresses

The special function Program Address allows you to set the base address into EEProm. This can be used within your factory to set device addresses before assembly or during ATE.

The EEProm WriteProtect bit, blocks any further changes except when a device is in special pins mode.

3.6.2 Using programmable addresses with ATE.

When building a system with many chips of the same type on the same bus, it is desirable to install identical chips, then change the addresses during the ATE phase. This can be done by using the RG (resistor to VSS) at each chip. The ATE system has a probe/pogo to connecting to each A0 pin and the common SCL,SDA. It pulls A0 to VSS, then rewrites that chips base address.

4 Table 2: Addresses and Commands

Char	Command		Chars to Follow		
	direct tristate				
	pwm value				
	pwm period				
	set flags				
	set I2C Base Address				

	reset				
	sleep				

5 Command Format

Unrecognised chars are generally ignored[3].
Chars are generally processed and acted on immediately.
The basic form follows that shown in the Philips I2C documentation.

5.1 A simple I2C Transaction

f			
Bit	Rst	Name	Description
3	1		
1	0		

6 EEProm Settings

7			
6			
5			
4			
3			
2			
1	EESleepWhenIdle		Sleeps when Idle. Can't use when using contrast voltage
0	EEWrProtect		

7 Oscillator

8 Reset

8.1 Reset Time

Power on reset typically takes ?ms. The BLXX will not respond to commands until after this period.

8.2 Software reset

8.2.1 GCA and SMBus Reset

These parts do not respond to the Global Call address or other special SMBus addresses.

[3] Spaces and Commas are always ignored. You may freely use them to make strings more readable (if slower). You can use CR and/or LF if you wish.

8.3 I2C Address

The I2C Address pin is read at power on. Changing its state after power on will be ignored.

9 Sleep Mode

The BLXX enters sleep mode between commands, and wakes up automatically on I2C transactions

10 I2C Bus Connectors and Pinouts

We use this pinout, and recommend that you do also. More details, and connector part#'s, suppliers etc see: http://www.i2cchip.com/i2c_connector.html

Pin#	6 Way	4 Way	
1	SDA	SDA	
2	+5	+5	
3	Gnd	Gnd	
4	SCL	SCL	
5	INT		Interrupt input (active low). Can be used as CS when being used for an SPI bus.
6	VAux		Aux supply (eg 12V), or other uses.

11 Example Applications

12 Errata & Migration

13 Ordering Information

We recommend buying one built up module to save time and hassles.
DIP parts are available in low volume. SOIC and SSOP20 parts are only available for volume orders at this time.
DIP18: BLXX-P
SO18W: BLXX-D
SSOP20: BLXX-M

EEProm settings can be customised at the factory for high volume

14 Co-operation

We offer all customers a link page on our web site, where others can find out about ***your*** products. We encourage you to use this.